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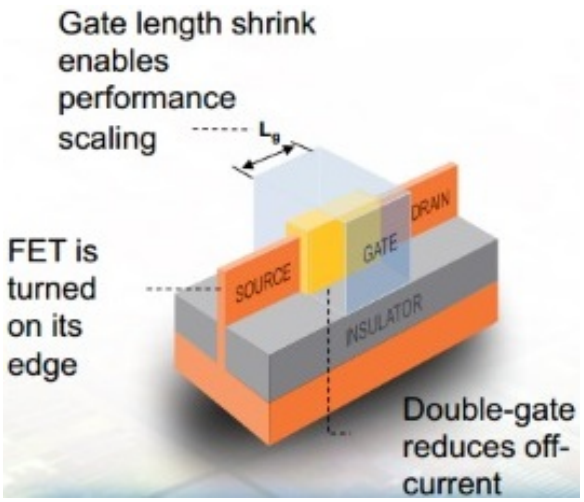
Infringement Chart for U.S. Patent No. 6,885,055

Claim 1	Accused Instrumentalities
A double-gate FinFET device, comprising:	The Accused Instrumentality comprises a double-gate FinFET device. For example, Defendants Samsung and GloFo provide the following graphic.[1]  "In FinFET transistor [*sic*], the gate is placed on multiple sides of each source and drain, controlling the current leakage more effectively."[2] According to Defendant Samsung: "This platform . . . allows us to manufacture the highest performing, most energy efficient chips required for tomorrow's computing needs. For the first time, production with the most advanced 14nm FinFET technology will be available at multiple locations in the U.S. and Korea to meet the growing supply demands of our customers. As a result of this strategic collaboration, true design compatibility will reside in Korea, Texas and New York."[3] "In leading mass production of advanced FinFET logic process, Samsung announced in Q1 of 2015

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	the launch of the Exynos 7 Octa processor built on the industry's first 14nm LPE (Low-Power Early) process."[4] On January 14, 2016, Defendant Samsung announced, "mass production of advanced logic chips utilizing its 14nm LPP (Low-Power Plus) process, the 2nd generation of the company's 14nm FinFET process technology."[5] "With the new 14nm LPP process, Samsung continues to demonstrate its process technology leadership, and unparalleled performance and power efficiency for its Exynos 8 Octa processor and its many foundry customers including Qualcomm Technologies, Inc. The Qualcomm® Snapdragon™ 820 processor uses Samsung's new 14nm LPP process and is expected to be in devices in the first half of [2016]."[6] According to Charlie Bae, Executive Vice President of Sales & Marketing, System LSI Business, Samsung Electronics: "We are pleased to start production of our industry-leading, 2nd generation 14nm FinFET process technology that delivers the highest level of performance and power efficiency. Samsung will continue to offer derivative processes of its advanced 14nm FinFET technology to maintain our technology leadership."[7] The Accused Instrumentality incorporates a "three-dimensional (3D) FinFET structure on transistors [that] enables significant performance boost and low power consumption. Samsung's new 14nm LPP process delivers up to 15 percent higher speed and 15 percent less power consumption over the previous 14nm LPE process through improvements in transistor structure and process optimization. In addition, use of fully-depleted FinFET transistors brings enhanced manufacturing capabilities to overcome scaling limitations."[8] According to Defendant Samsung, "[t]he advantages to the 14nm FinFET platform is a result of utilizing 3D FinFET transistors to enable a 35% savings in power consumption compared to 20nm planar technology without sacrificing performance. It also can be tuned for high-performance wired applications for a 20% boost in output at constant power."[9] For example, according to Defendant Samsung, "[w]ith 14nm FinFET process technology, Exynos 7870 consumes up to 30% less power than its predecessor built on 28nm HKMG process at the same performance level. With 14nm FinFET process, octa-core 64-bit CPUs offer a perfect balance between performance and power efficiency."[10]

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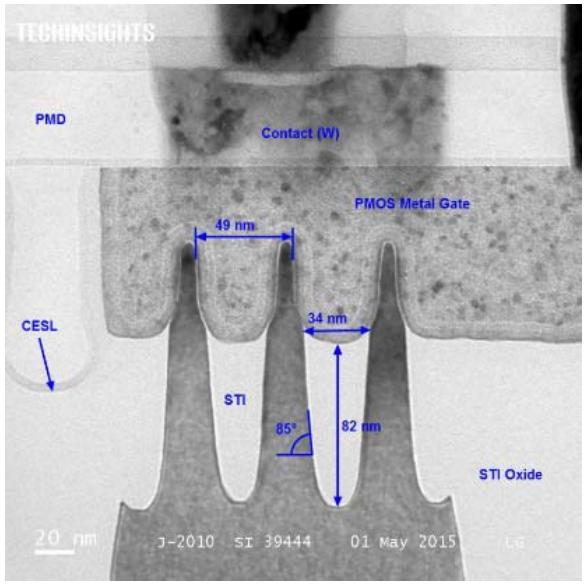
	The following image shows an example of the Accused Instrumentality.[11]  "The Exynos 7420 is Samsung's first 14 nm bulk finFET based application processor that is adopted in the Samsung's Galaxy S6 smartphone. The Exynos 7420 is a 64 bit octa-core processor with ARM big.LITTLE architecture which contains 2.1 GHz quad core Cortex A57 and 1.5 GHz quad core Cortex A53 CPUs, ARM Mali-T760MP8 GPU, and LPDDR4 as a memory interface. The Exynos 7420 is fabricated by a 14 nm process technology adopting finFET architecture with 12 levels of metallization (10 Cu, 1 Al, and 1 W), and a high-k dielectric replacement metal gate (HKMG) process on a bulk silicon substrate. The transistor's channel, source and drain regions are formed on a silicon fin protruding from the substrate, with the gate wrapped around three sides of the fin. The isolation trenches are likely formed using a two different depth etch process to facilitate the better isolation between adjacent finFET devices (set of fins) with deeper isolation trenches. A high-k gate dielectric (HfO) with a SiO2 interfacial layer are used as a gate dielectric for PMOS and NMOS transistors that use different metal gates. PMOS metal gate stacks consist of AlTiN

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	work function adjustment layer, AlTiC, metal oxide (likely AlTiO), TiN capping layer and W gate filling metal. W is not filled in the narrow space of gate trenches in standard logic PMOS transistors including SRAM PMOS pull-up transistors. AlTiN PMOS work function layer is likely removed from NMOS transistors prior to depositing NMOS work function adjustment layer (AlTiC). NMOS metal gate stacks start with remnant AlTiN PMOS work function layer, AlTiC NMOS work function layer, metal oxide (likely AlTiO), TiN capping layer and W gate filling metal. The finFET channel is oriented to the <110> directions with minimum gate length 27 nm for PMOS transistor and 30 nm for NMOS transistor in logic region. Embedded SiGe in PMOS source/drain regions apply compressive strain to transistor P-channel to increase holes' mobility and improve transistor performance. Lower seven levels of copper metallization employ similar dense metal line with a fine pitch indicating 1x routing and minimum metal pitch in 1x routing levels is observed at metal 2 level as 67 nm of pitch. The device features a 78 nm minimum observed contacted gate pitch, 49 nm minimum observed fin pitch and 0.08 μm2 minimum observed 6T SRAM cell area."[12] "The Samsung Exynos 7420 application processor die is fabricated using a 12 metal layer including metal 0, replacement metal gate, 14 nm bulk finFET CMOS process. The device features a lightly doped p-type bulk silicon substrate having a <110> channel orientation, hafnium oxide/silicon oxide gate dielectric, dual band edge work function metal gates, tungsten contacts and metal 0, 10 levels of copper metallization, aluminum top metal (metal 11) redistribution layer and carbon-doped low-k dielectric (SiOC) inter-level dielectrics. A dual damascene copper process is used for all interconnect levels except for metal 0 (W) and metal 11 (Al)."[13] In April 2014, Defendants Samsung and GloFo announced "a new strategic collaboration to deliver global capacity for 14 nanometer (nm) FinFET process technology. For the first time, the industry's most advanced 14nm FinFET technology will be available at both Samsung and GLOBALFOUNDRIES, giving customers the assurance of supply that can only come from true design compatibility at multiple sources across the globe. The new collaboration will leverage the

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	companies' worldwide leading-edge semiconductor manufacturing capabilities, with volume production at Samsung's fabs in Hwaseong, Korea and Austin, Texas, as well as GLOBALFOUNDRIES' fab in Saratoga, New York." Upon information and belief, GloFo and Qualcomm Chips utilize the same or substantially similar FinFET architecture as in the Exynos 7420 processors. "Now, thanks to a strategic collaboration with GLOBALFOUNDRIES, 14nm FinFET production capabilities will soon reach worldwide scale."[14]
a bulk silicon substrate;	The Accused Instrumentality comprises a bulk silicon substrate. Defendant Samsung's Exynos 7420 SoC "is fabricated by a 14 nm process technology adopting finFET architecture with 12 levels of metallization (10 Cu, 1 Al, and 1 W), and a high-k dielectric replacement metal gate (HKMG) process on a bulk silicon substrate. The transistor's channel, source and drain regions are formed on a silicon fin protruding from the substrate, with the gate wrapped around three sides of the fin. The isolation trenches are likely formed using a two different depth etch process to facilitate the better isolation between adjacent finFET devices (set of fins) with deeper isolation trenches."[15] For example, the bulk silicon substrate is illustrated in the graphic below (left)[16] and shown in the image below (right).[17]

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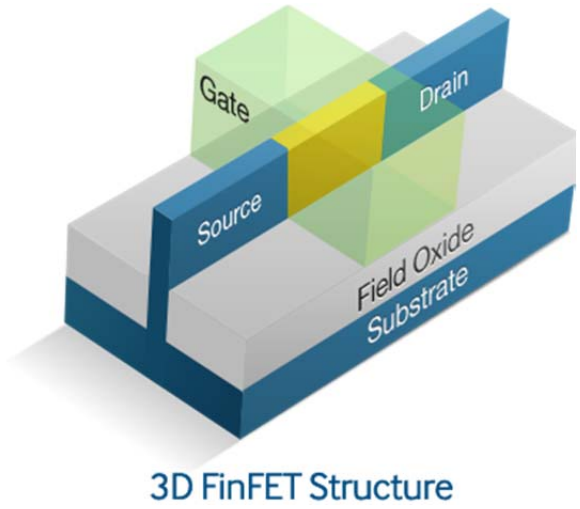
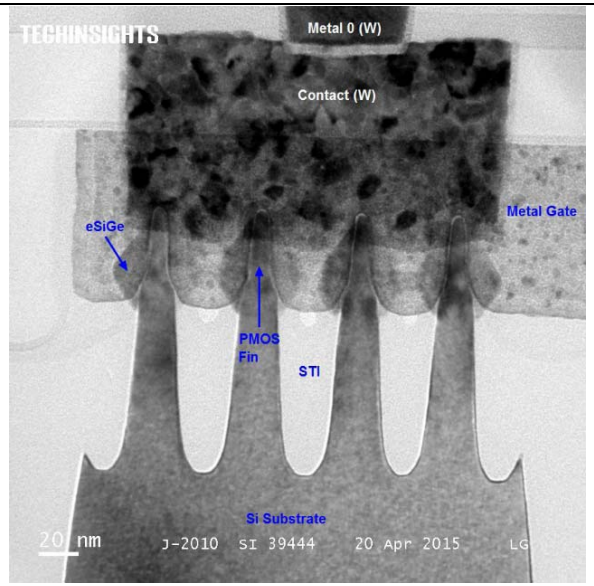
	 3D FinFET Structure 
a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate;	The Accused Instrumentality comprises a wall-shape single crystalline silicon Fin active region on a surface of the bulk silicon substrate and connected to the bulk silicon substrate. The Accused Instrumentality includes a Fin active region, on which the transistor's channel, source, and drain are located, formed on the bulk silicon substrate. "The Exynos 7420 is fabricated by a 14 nm process technology adopting finFET architecture with 12 levels of metallization (10 Cu, 1 Al, and 1 W), and a high-k dielectric replacement metal gate (HKMG) process on a bulk silicon substrate. The transistor's channel, source and drain regions are formed on a silicon fin protruding from the substrate, with the gate wrapped around three sides of the fin. The isolation trenches are likely formed using a two different depth etch process to facilitate the better isolation between adjacent finFET devices (set of fins) with deeper isolation trenches."[18] The Fin active region of the infringing device is comprised of single crystalline silicon. "The Samsung Exynos 7420 application processor is fabricated using a lightly doped bulk P-type monocrystalline Si substrate."[19]

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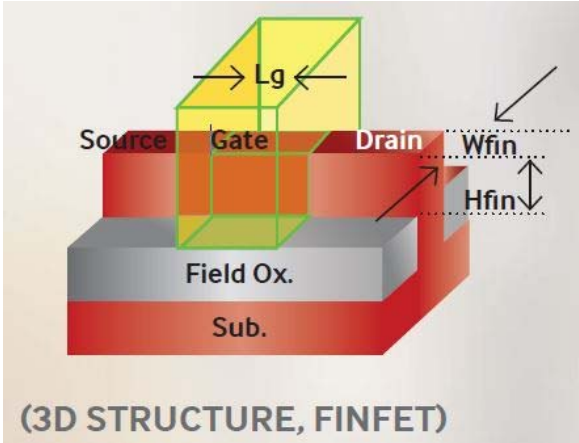
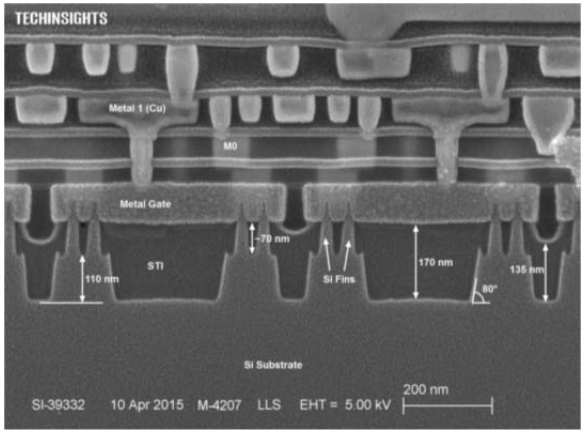
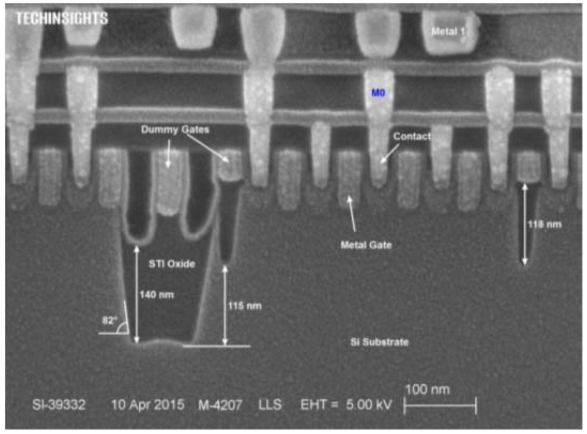
For example, these features are illustrated in the graphic below.[20]



They are also shown in the images below.[21]





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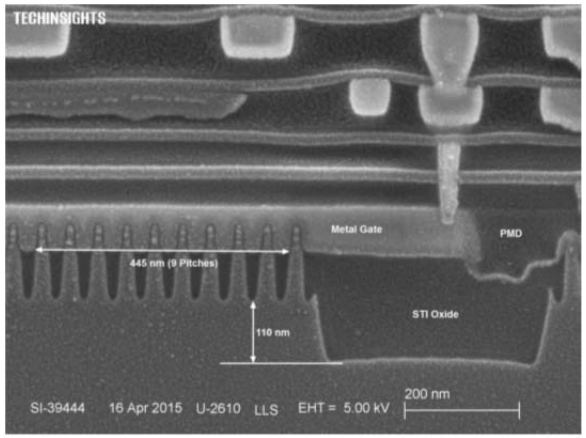

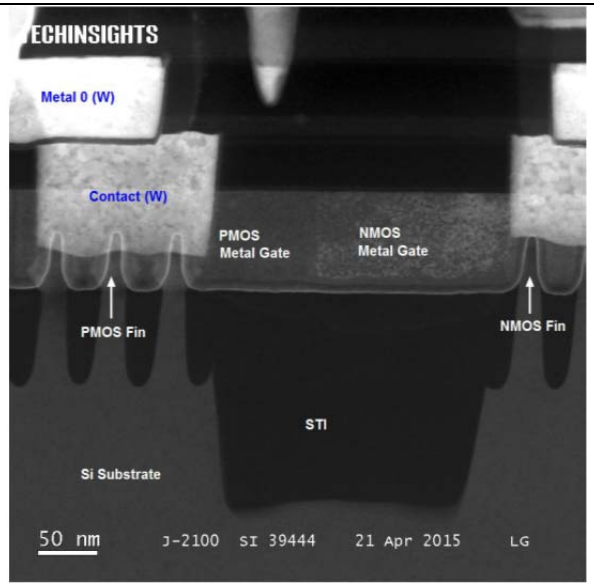

The Fin active regions of the infringing devices are wall-shaped. "A two-step etch process is used to define the fins and STIs. The fins are patterned by a 1st shallow trench isolation etch. A second etch is used to form the deep STI trenches between adjacent fin structures. The fins are likely formed using a sacrificial pad mask with a double patterning process (likely SADP, self-aligned double patterning)."[22]

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	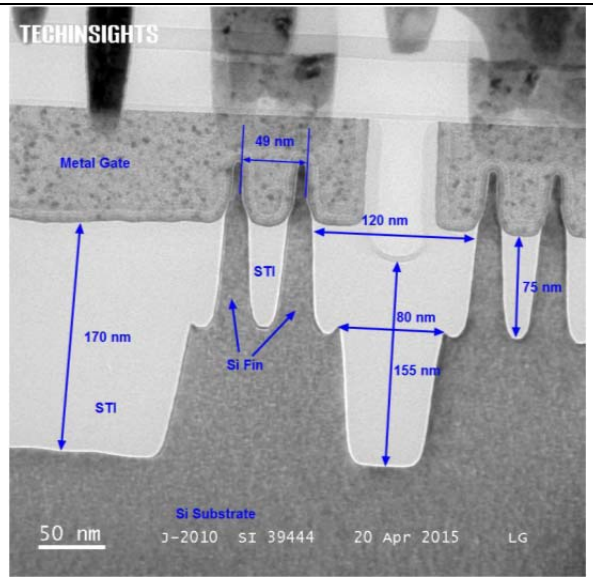 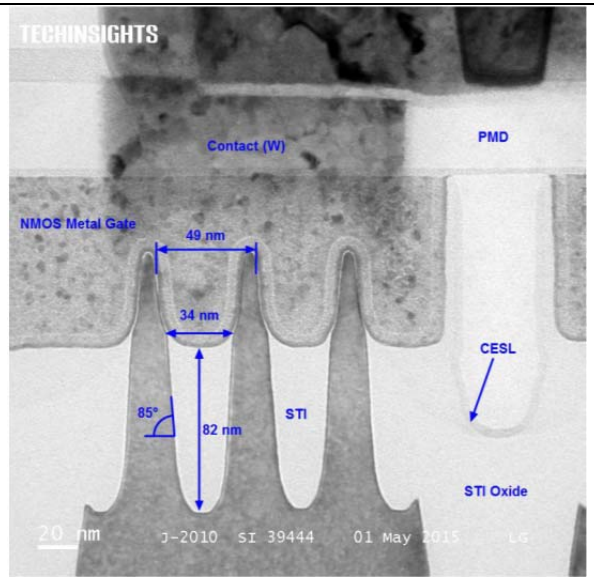 The Fin active region is wall-shaped, monocrystalline silicon, and connected to the bulk silicon substrate.
a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;	The Accused Instrumentality comprises a second oxide layer, which is formed up to a certain height of the Fin active region, from the surface of bulk silicon substrate. For example, the second oxide layer (*i.e.*, Field Oxide) feature is illustrated in the graphic below.[23]

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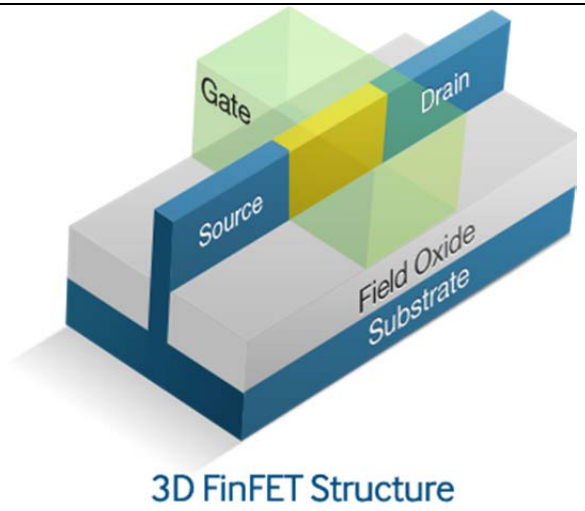
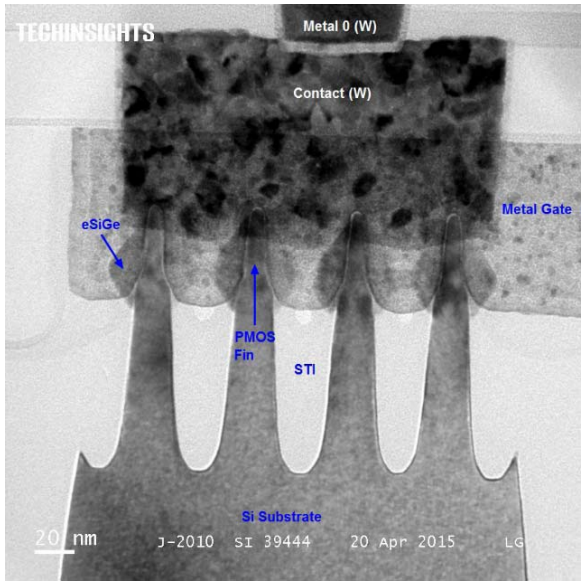
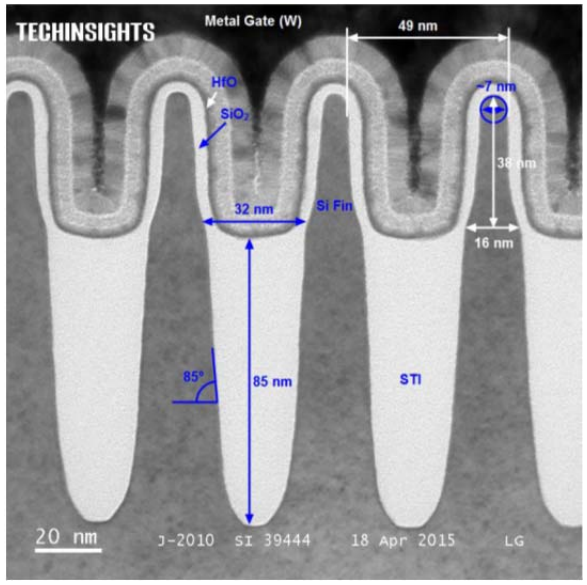


It also shown in the images below.[24]





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	A second oxide layer is formed up to a desired height on the Fin active regions, on which a gate is formed. "The Samsung Exynos 7420 uses shallow trench isolation (STI) to provide isolation between the fin structures (devices) on the die and the trenches are filled with a single oxide (SiO2). . . . After completion of deeper STI formation, the trenches are filled with oxide (SiO2) and CMP planarized. The STI oxide fill is then etched back to expose the fins."[25] The second oxide layer is formed up from the surface of the bulk silicon substrate to a certain height of the Fin active region.
a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer;	The Accused Instrumentality comprises a gate oxide layer, which is formed on both side-walls of the Fin active region, protruded from said second oxide layer. A high-κ dielectric is formed on the side-walls of the Fin active region, creating the gate oxide layer. "A high-k dielectric including thin interface oxide separates the fin from the metal gate on each of the three sides of the fin. The gate dielectric consists of ~0.8 nm interface dielectric SiO2 and ~1.2 nm high-k dielectric HfO. The I/O transistor is observed to have a thicker interface dielectric SiO2 as compared to the standard logic transistor. The metal gates are constrained to be parallel in one direction (across the fin direction) and have a contacted gate pitch about 78 nm and minimum gate length of 27 nm for PMOS and 30 nm for NMOS in standard logic area."[26] For example, the gate oxide layer is illustrated in the graphic below[27]

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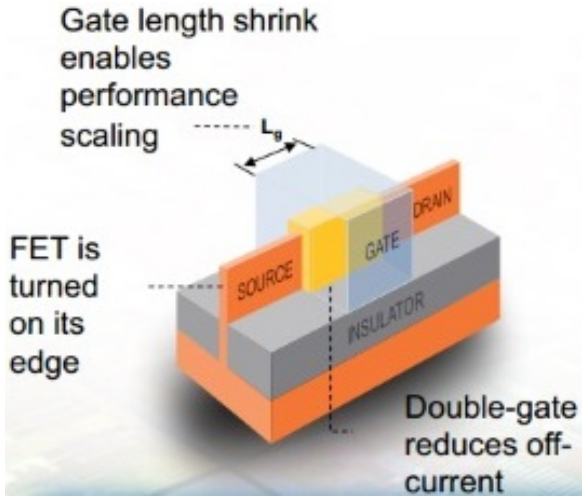
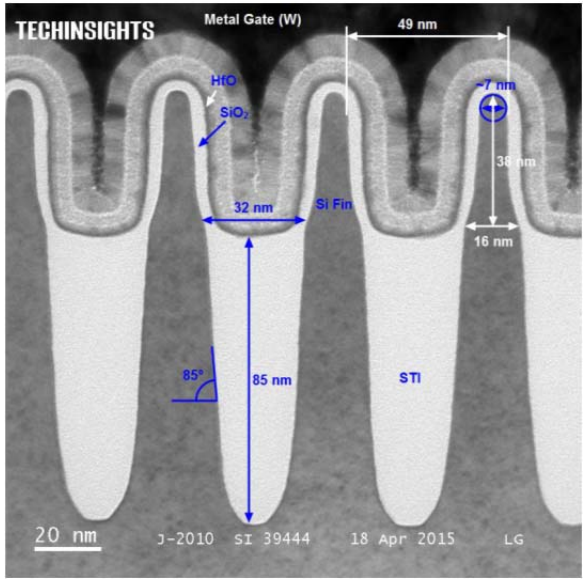
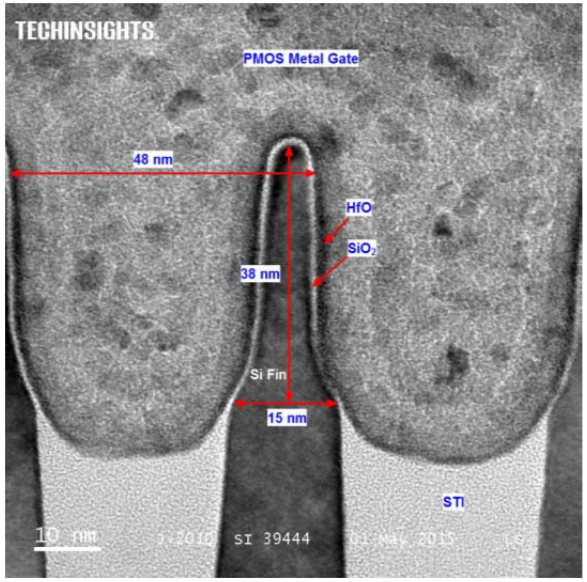


It is also shown in the images below.[28]





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	"After removing sacrificial poly-Si gate, the gate dielectric layer is formed along the sidewall and a bottom surface of gate trench. The gate dielectric includes interface oxide (SiO2) and high-k dielectric (HfO) likely grown by ALD process."[29] The gate oxide layer is formed on both side-walls of the Fin active region.
a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide;	The Accused Instrumentality comprises a first oxide layer, which is formed on the upper surface of the Fin active region, with a thickness greater or equal to that of the gate oxide. A first oxide layer is formed on the upper surface of the Fin active region from a high-κ dielectric. "A high-k dielectric including thin interface oxide separates the fin from the metal gate on each of the three sides of the fin. . . . The I/O transistor is observed to have a thicker interface dielectric SiO2 as compared to the standard logic transistor."[30] For example, the first oxide layer, shown in the image below, has a thickness greater than or equal to the thickness of the gate oxide.[31]

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	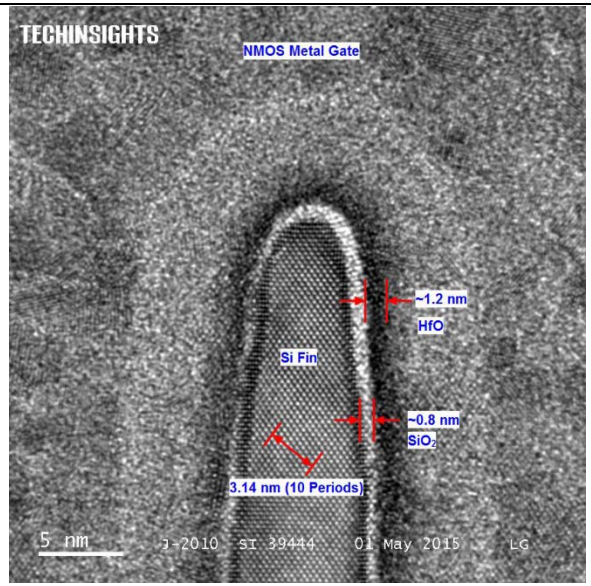
a gate which is formed on said first and second oxide layer;	The Accused Instrumentality comprises a gate, which is formed on the first and second oxide layers. A metal gate wraps around the sides and top of the Fin active region. "The Exynos 7420 is fabricated by a 14 nm process technology adopting finFET architecture with . . . a high-k dielectric replacement metal gate (HKMG) process on a bulk silicon substrate. The transistor's channel, source and drain regions are formed on a silicon fin protruding from the substrate, with the gate wrapped around three sides of the fin."[32] "The Samsung Exynos 7420 application processer is fabricated using Samsung's 1st generation finFET process technology in which a gate is wrapped around a thin three-dimensional silicon fin. The device employs multi-layered metal gates using a gate last process (RMG-replacement metal gate), epitaxial Si in the source/drains (S/D) of the NMOS finFETs and epitaxial silicon germanium (e-SiGe) in the PMOS S/Ds. Dual work function metal gates are used for PMOS and NMOS finFETs. A high-k dielectric including thin interface oxide separates the fin from the metal

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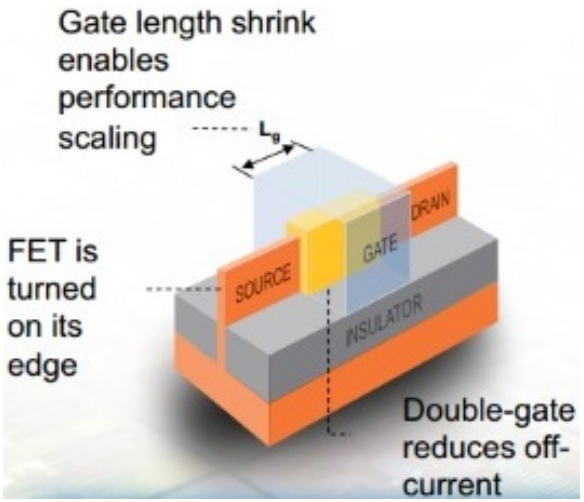
	gate on each of the three sides of the fin. The gate dielectric consists of ~0.8 nm interface dielectric SiO2 and ~1.2 nm high-k dielectric HfO. The I/O transistor is observed to have a thicker interface dielectric SiO2 as compared to the standard logic transistor. The metal gates are constrained to be parallel in one direction (across the fin direction) and have a contacted gate pitch about 78 nm and minimum gate length of 27 nm for PMOS and 30 nm for NMOS in standard logic area."[33] For example, the gate is illustrated in the graphic below.[34]  It is also shown in the images below.[35]

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	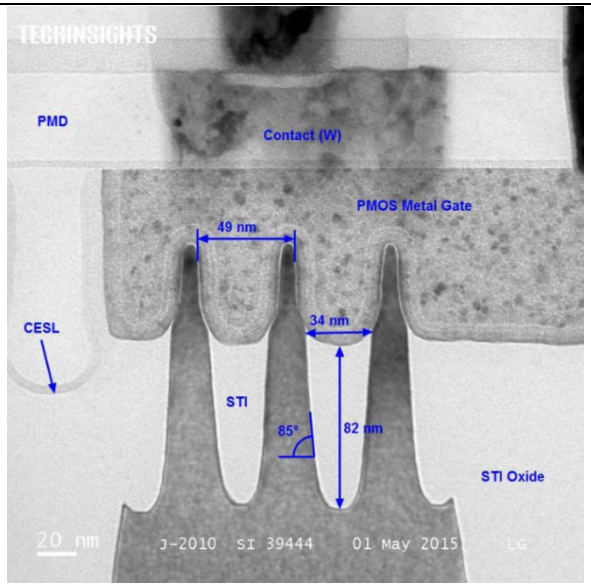 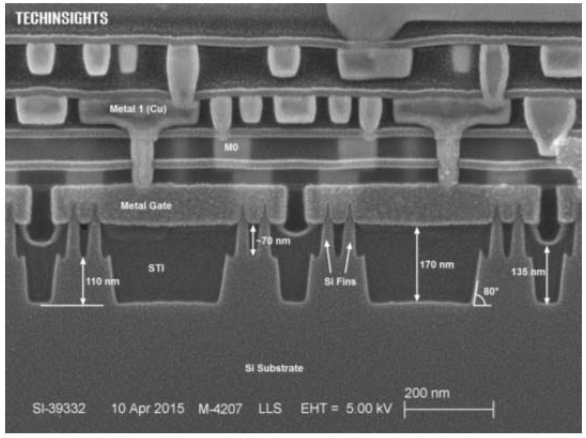 The gate is formed on the first and second oxide layers.
a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and	The Accused Instrumentality comprises a source/drain region formed on both sides of the Fin active region, except where said gate overlaps with the Fin active region. "The transistor's channel, source and drain regions are formed on a silicon fin protruding from the substrate . . . ."[36] "Source/drain regions of NMOS finFETs are anisotropically etched to form recess in the fin and embedded Si (eSi) is formed by selective epitaxial growth. The shape of eSi is more rounded compared to the diamond shaped eSiGe in PMOS source/drain regions."[37] For example, the source/drain region is depicted on both sides of the Fin active region, except where the gate overlaps the Fin active region, both in the graphic below (left)[38] and in the image below (right).[39]

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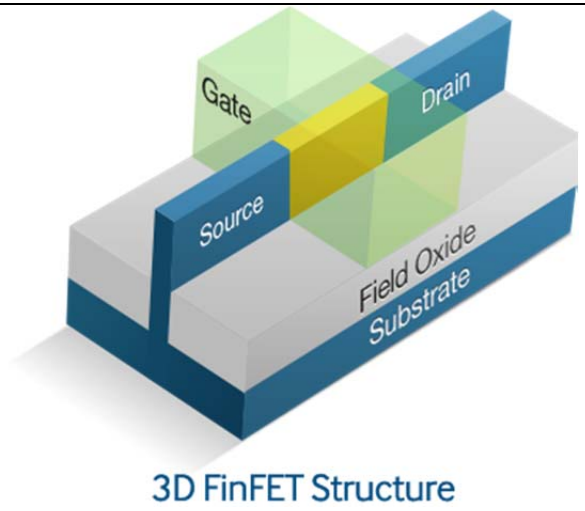
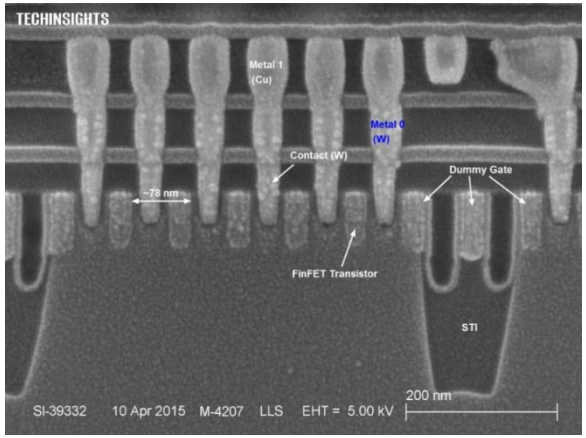
	 3D FinFET Structure 
a contact region and a metal layer which are formed at said source/drain and gate contact region,	The Accused Instrumentality comprises a contact region and a metal layer, which are formed at said source/drain and gate contact region. For example, the Accused Instrumentality "is fabricated using a 12 metal layer including metal 0, replacement metal gate, 14 nm bulk finFET CMOS process. The device features a lightly doped p-type bulk silicon substrate having a <110> channel orientation, hafnium oxide/silicon oxide gate dielectric, dual band edge work function metal gates, tungsten contacts and metal 0, 10 levels of copper metallization, aluminum top metal (metal 11) redistribution layer and carbon-doped low-k dielectric (SiOC) inter-level dielectrics. A dual damascene copper process is used for all interconnect levels except for metal 0 (W) and metal 11 (Al)."[40] As can be seen in the images below, the Accused Instrumentality includes contact regions and metal layers, which are formed at various source/drain and gate contact regions.[41]

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	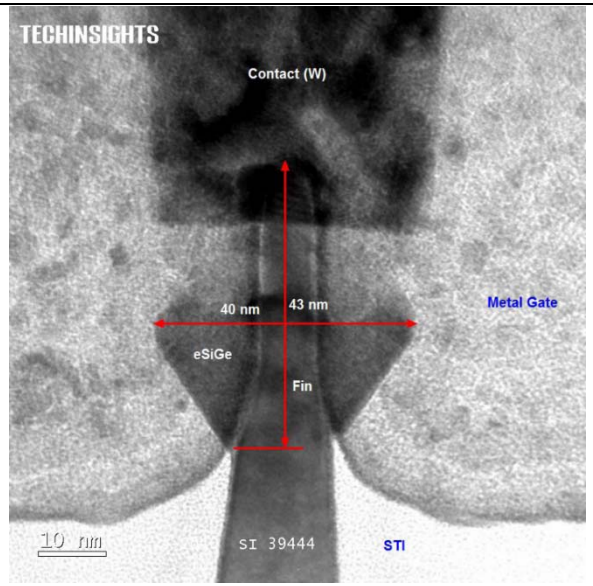 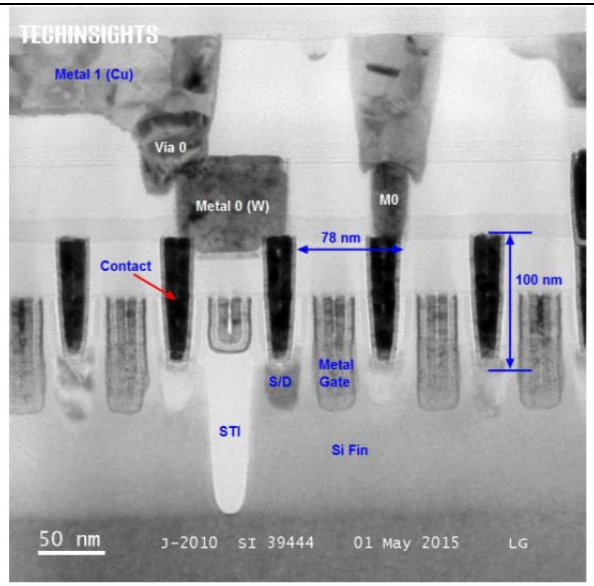
wherein the thickness of said gate oxide layer is between 0.5 nm and 10 nm, and the thickness of said first oxidation layer is between 0.5 nm and 200 nm.	In the Accused Instrumentality, the thickness of the gate oxide layer is between 0.5 nm and 10 nm, and the thickness of the first oxidation layer is between 0.5 nm and 200 nm. For example, in the Accused Instrumentality, "[a] high-k dielectric including thin interface oxide separates the fin from the metal gate on each of the three sides of the fin. The gate dielectric consists of ~0.8 nm interface dielectric SiO2 and ~1.2 nm high-k dielectric HfO."[42] As shown in the image below, the gate oxide layer and first oxidation layer thicknesses employed in the Accused Instrumentality are between 0.5 nm and 10 nm, and between 0.5 nm and 200 nm, respectively.[43]

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	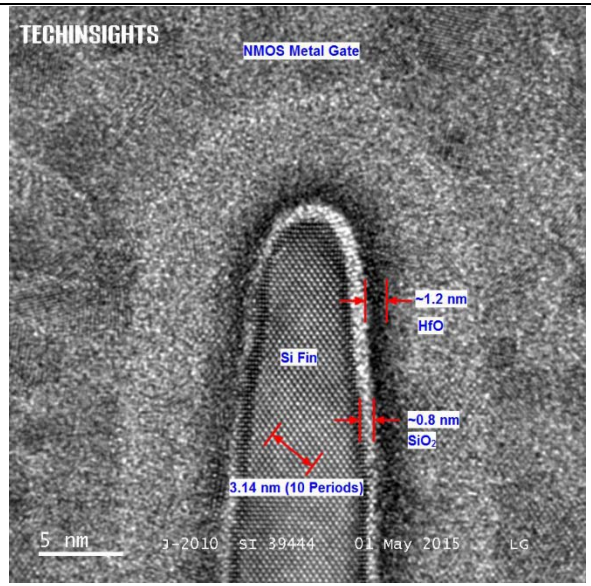

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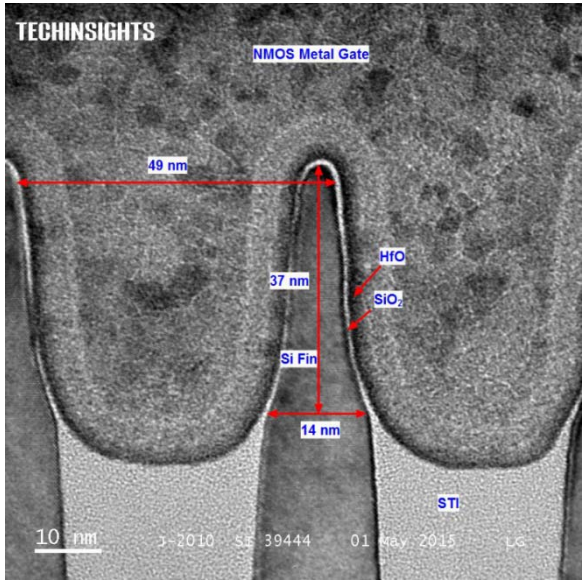
Claim 2	Accused Instrumentalities
The device as claimed in claim 1, wherein the width of said Fin active region lies in a range between 4 nm and 100 nm.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the Fin active region has a width that lies in a range between 4 nm and 100 nm. For example, as shown below, the width of the Fin active region lies in a range between 4 nm and 100 nm.[44] 

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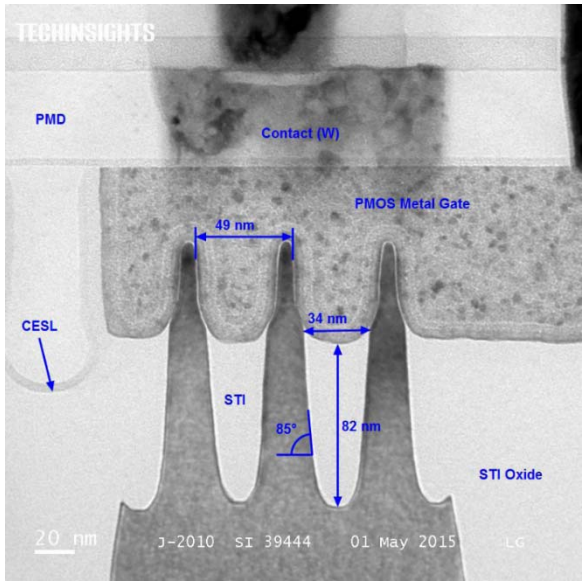
Claim 3	Accused Instrumentalities
The device as claimed in claim 1, wherein the height of said Fin active region from the surface of said bulk silicon substrate lies in a range between 10 nm and 1000 nm.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the Fin active region has a height from the surface of the bulk silicon substrate that lies in a range between 10 nm and 1000 nm. For example, as shown below, the height of the Fin active region from the surface of the bulk silicon substrate lies in a range between 10 nm and 1000 nm.[45] 

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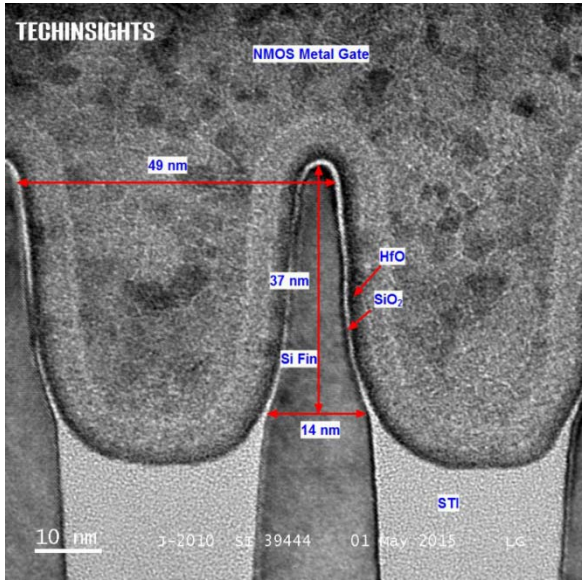
Claim 4	Accused Instrumentalities
The device as claimed in claim 3, wherein the height of said Fin active region from the surface of said second oxide layer is between 5 nm and 300 nm.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 3, in which the Fin active region has a height from the surface of the second oxide layer is between 5 nm and 500 nm. For example, as shown below, the height of the Fin active region from the surface of the second oxide layer is between 5 nm and 300 nm.[46] 

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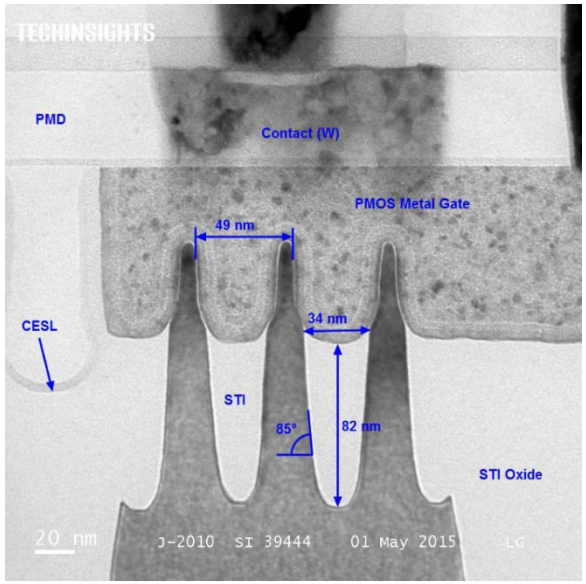
Claim 5	Accused Instrumentalities
The device as claimed in claim 1, wherein the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which thickness of the second oxidation layer is selected to be between 20 nm and 800 nm, reducing the parasitic capacitance between the gate and bulk silicon substrate. For example, the thickness of the second oxidation layer shown in the image below is between 20 nm and 800 nm.[47]  The design in the Samsung FinFET Technology reduces the parasitic capacitance between the gate and bulk silicon substrate.[48]

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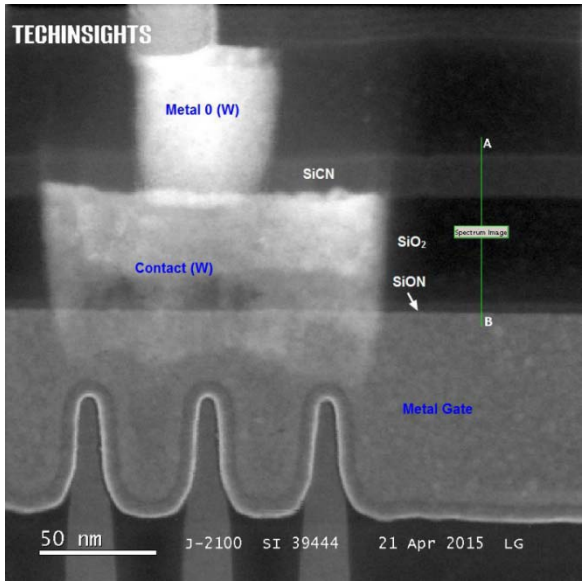
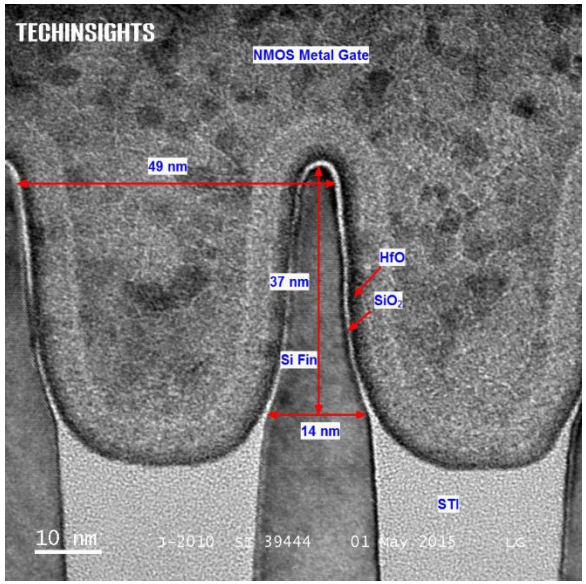
Claim 6	Accused Instrumentalities
The device as claimed in claim 1, wherein the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the size of the region in contact with the metal layer is selected to be greater than the width of the Fin active region and/or the length of the gate, reducing the contact resistance. For example, the size of a contact region which is in contact with the metal layer (below left) is greater than the width of the Fin active region (below right).[49] The design in the Samsung FinFET Technology reduces the contact resistance.  

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Claim 7	Accused Instrumentalities
A double-gate FinFET device, comprising:	*See* Claim 1, with respect to same preamble, page 1.
a bulk silicon substrate;	*See* Claim 1, with respect to same element/limitation, page 5.
a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate;	*See* Claim 1, with respect to same element/limitation, page 6.
a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;	*See* Claim 1, with respect to same element/limitation, page 9.
a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer;	*See* Claim 1, with respect to same element/limitation, page 11.
a first oxide layer which is formed on the upper surface of said Fin active region with a	*See* Claim 1, with respect to same element/limitation, page 13.

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thickness greater or equal to that of the gate oxide;	
a gate which is formed on said first and second oxide layer;	*See* Claim 1, with respect to same element/limitation, page 14.
a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and	*See* Claim 1, with respect to same element/limitation, page 16.
a contact region and a metal layer which are formed at said source/drain and gate contact region,	*See* Claim 1, with respect to same element/limitation, page 17.
wherein the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region, and/or the length of said gate,	*See* Claim 6, with respect to same element/limitation, page 24.
and selective epitaxial layer is grown on both sides (source/drain region) of the Fin	The Accused Instrumentality comprises a selective epitaxial layer, grown on both sides of the Fin active region except where the Fin active region overlaps with the gate in a self-aligned manner to

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active region except where said Fin active region overlaps with the gate in a self-aligned manner to the gate, in order to reduce parasitic source/drain resistance.	the gate, in order to reduce parasitic source/drain resistance. For example, the Accused Instrumentality "is fabricated using Samsung's 1st generation finFET process technology in which a gate is wrapped around a thin three-dimensional silicon fin. The device employs multi-layered metal gates using a gate last process (RMG-replacement metal gate), epitaxial Si in the source/drains (S/D) of the NMOS finFETs and epitaxial silicon germanium (e-SiGe) in the PMOS S/Ds. Dual work function metal gates are used for PMOS and NMOS finFETs. A high-k dielectric including thin interface oxide separates the fin from the metal gate on each of the three sides of the fin. The gate dielectric consists of ~0.8 nm interface dielectric SiO2 and ~1.2 nm high-k dielectric HfO. The I/O transistor is observed to have a thicker interface dielectric SiO2 as compared to the standard logic transistor. The metal gates are constrained to be parallel in one direction (across the fin direction) and have a contacted gate pitch about 78 nm and minimum gate length of 27 nm for PMOS and 30 nm for NMOS in standard logic area. . . . Strain silicon techniques for stressing the transistor channels are employed including SEG (selective epitaxial growth) layers in the S/Ds such as embedded SiGe (eSiGe) in PMOS and embedded Si (eSi) in NMOS. NMOS devices are assumed to have a tensile stress in the channels of the transistors while PMOS transistors are assumed to include a compressive stress in the channel. Transistors are aligned to the <110> substrate channel orientation. The sidewall structures of both PMOS and NMOS transistors are made of SiOCN deposited conformably and etched back anisotropically to make gate spacers."[50] The selective epitaxial layers in the Accused Instrumentality is shown below.[51]

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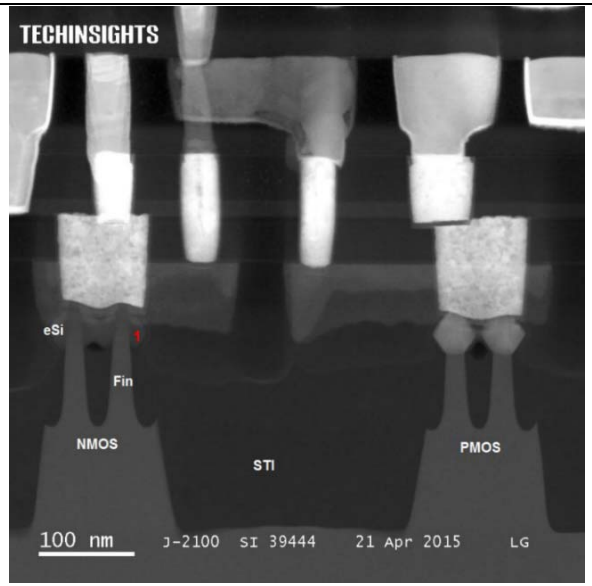

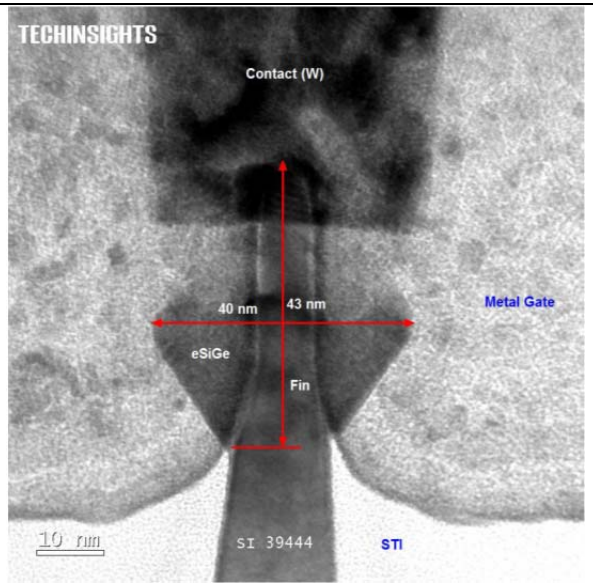

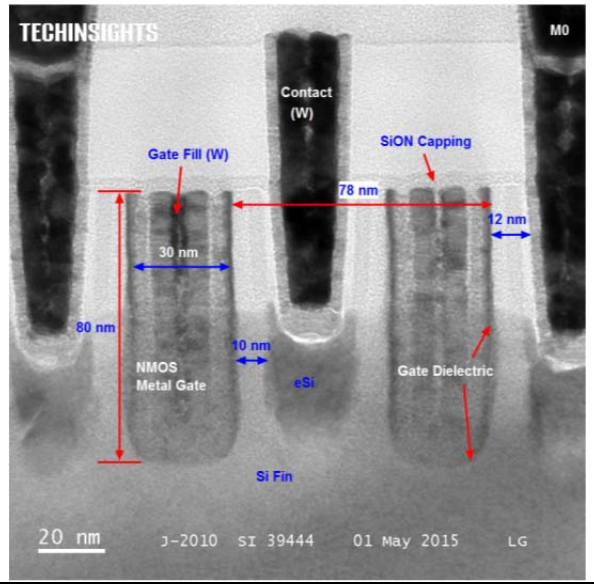

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	The epitaxial layers are located on both sides (source/drain region) of the Fin active region except where the Fin active region overlaps with the gate, in a self-aligned manner to the gate.[52] The use of the selective epitaxial layers in this manner reduces parasitic source/drain resistance.

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Claim 9	Accused Instrumentalities
The device as claimed in claim 7, wherein said selective epitaxial layer is grown by depositing a dielectric layer, and anisotropically etching as much as the thickness of the dielectric layer and the height of the Fin active region protruding above the second oxide layer, and taking the silicon which is exposed at side-walls of the Fin active region except the vicinity where the Fin active region and gate meets and a poly-silicon gate, as seeds.	Upon information and belief, the Accused Instrumentality comprises a FinFET device, as claimed in claim 7, in which the selective epitaxial layer is grown by depositing a dielectric layer, and anisotropically etching as much as the thickness of the dielectric layer and the height of the Fin active region protruding above the second oxide layer, and taking the silicon which is exposed at side-walls of the Fin active region except the vicinity where the Fin active region and gate meets and a poly-silicon gate, as seeds. Discovery is expected to uncover additional evidence of infringement of claim 9 by the Accused Instrumentalities.

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Claim 10	Accused Instrumentalities
The device as in any one of claims 7, wherein the material for said selective epitaxial layer is selected from the group consisting of a single crystalline silicon, single crystalline SiGe, single crystalline Ge, poly-silicon, and poly SiGe.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 7, in which the material for the selective epitaxial layer is selected from the group consisting of a single crystalline silicon, single crystalline SiGe, single crystalline Ge, poly-silicon, and poly SiGe. For example, in the Accused Instrumentality, "[s]train silicon techniques for stressing the transistor channels are employed including SEG (selective epitaxial growth) layers in the S/Ds such as embedded SiGe (eSiGe) in PMOS and embedded Si (eSi) in NMOS."[53]

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Claim 11	Accused Instrumentalities
The device as claimed in claim 1, wherein said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level.	Upon information and belief, the Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the doping junction depth for the source/drain formed in said Fin active region, when the upper surface of the second oxide layer is taken as a reference level of 0 nm, is around 0 nm to 50 nm above the reference level. Discovery is expected to uncover additional evidence of infringement of claim 11 by the Accused Instrumentalities.

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Claim 12	Accused Instrumentalities
The device as claimed in claim 1, wherein said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to -50 nm below the reference level.	Upon information and belief, the Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the doping junction depth for the source/drain formed in the Fin active region, when the upper surface of said second oxide layer is taken as a reference level of 0 nm, is around 0 nm to -50 nm below the reference level. Discovery is expected to uncover additional evidence of infringement of claim 12 by the Accused Instrumentalities.

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Claim 13	Accused Instrumentalities
A double-gate FinFET device, comprising:	*See* Claim 1, with respect to same preamble, page 1.
a bulk silicon substrate;	*See* Claim 1, with respect to same element/limitation, page 5.
a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate;	*See* Claim 1, with respect to same element/limitation, page 6.
a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;	*See* Claim 1, with respect to same element/limitation, page 9.
a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer;	*See* Claim 1, with respect to same element/limitation, page 11.
a first oxide layer which is formed on the upper surface of said Fin active region with a	*See* Claim 1, with respect to same element/limitation, page 13.

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thickness greater or equal to that of the gate oxide;	
a gate which is formed on said first and second oxide layer;	*See* Claim 1, with respect to same element/limitation, page 14.
a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and	See Claim 1, with respect to same element/limitation, page 16.
a contact region and a metal layer which are formed at said source/drain and gate contact region,	*See* Claim 1, with respect to same element/limitation, page 17.
wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate.	In the Accused Instrumentality, the width of the Fin active region is enlarged as it approaches the bulk silicon substrate within the oxidation layer, reducing the resistance of the Fin active region. For example, in the Accused Instrumentality, this feature is shown in the image below.[54]

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	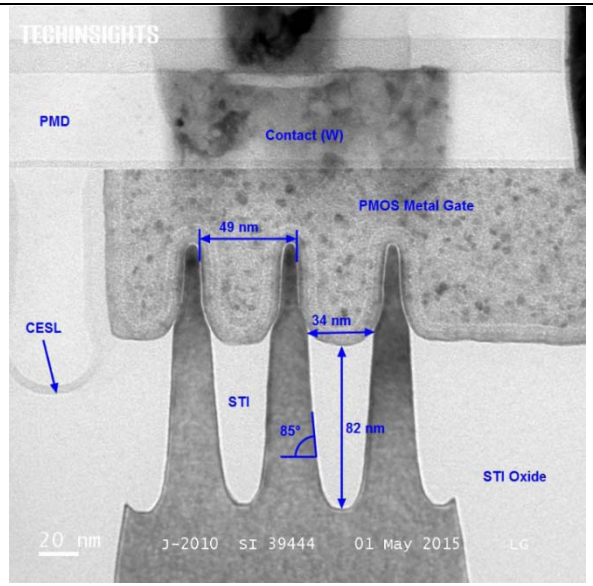 The width of the Fin active region increases as it approaches the bulk silicon substrate within the oxidation layer. The design in the Samsung FinFET Technology reduces the resistance of the Fin active region.

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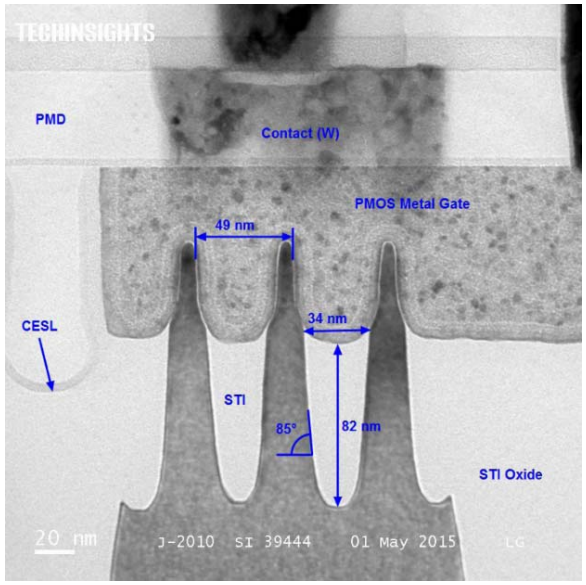
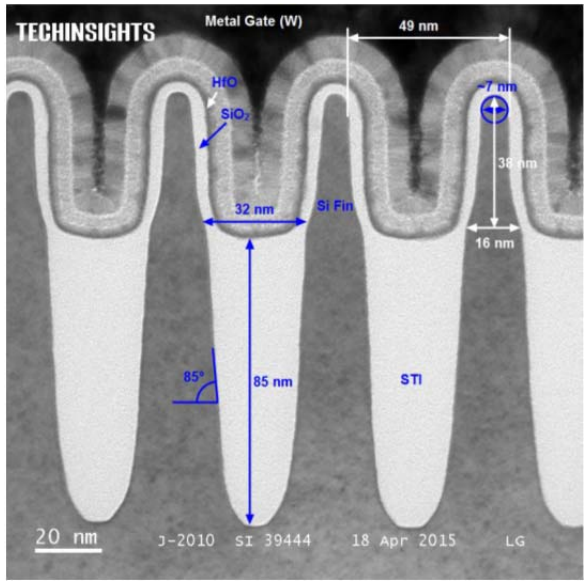
Claim 14	Accused Instrumentalities
The device as claimed in claim 1, wherein the shape of said Fin active region is a trapezoid where the width of the upper section is narrow and the lower section is wide.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the shape of the Fin active region is a trapezoid where the width of the upper section is narrow and the lower section is wide. For example, the width of the Fin active region shown in the image below is narrow in the upper section and wide in the lower section, in a trapezoidal shape (see below).[55]  

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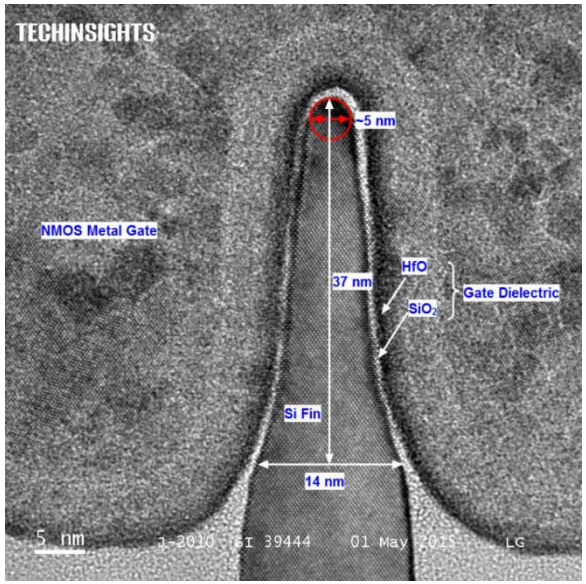
Claim 15	Accused Instrumentalities
The device as claimed in claim 1, wherein the two top corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere.	The Accused Instrumentality comprises a FinFET device, as claimed in claim 1, in which the top corners of the Fin active region are chamfered through oxidation and etching and/or annealing process in a hydrogen atmosphere.[56] For example, the two top corners of the Fin active region shown in the Accused Instrumentality are "rounded and thinned," as shown below.[57]  "Rounding the fins improves transistor performance by reducing the probability of TDDB (time dependent dielectric breakdown) due to sharp corners and increased electric fields. Thinned fin might provide better electrostatic control from the metal gate."[58]

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Claim 16	Accused Instrumentalities
The device as claimed in claim 2, wherein the height of said Fin active region from the surface of said bulk silicon substrate lies in a range between 10 nm and 1000 nm.	*See* Claim 3, with respect to same element/limitation, page 21.

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Claim 17	Accused Instrumentalities
The device as claimed in claim 16, wherein the height of said Fin active region from the surface of said second oxide layer is between 5 nm and 300 nm.	*See* Claim 4, with respect to same element/limitation, page 22.

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Claim 19	Accused Instrumentalities
The device as claimed in claim 9, wherein the material for said selective epitaxial layer is selected from the group consisting of a single crystalline silicon, single crystalline SiGe, single crystalline Ge, poly-silicon, and poly SiGe.	*See* Claim 10, with respect to same element/limitation, page 31.

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[1] *Samsung-GlobalFoundries 14nm Collaboration*, GLOBALFOUNDRIES (Apr. 2014), http://globalfoundries.com/docs/default-source/PDF/samsung-globalfoundries-14nm-collaboration---final.pdf.

[2] *Exynos 8 Octa (8890)*, SAMSUNG, http://www.samsung.com/semiconductor/minisite/Exynos/w/solution/mod_ap/8890/ (last visited Sep. 16, 2016).

[3] Kelvin Low, *Not all FinFETs Are Created Equal*, SAMSUNG (Apr. 17, 2014), http://www.samsung.com/semiconductor/insights/article/20683/.

[4] *Samsung Announces Mass Production of 2nd Generation 14-Nanometer FinFET Logic Process Technology*, SAMSUNG (Jan. 14, 2016), http://www.samsung.com/semiconductor/about-us/news/24581/.

[5] *Id.*

[6] *Id.*

[7] *Id.*

[8] *Id.*

[9] Low, *supra* note 3.

[10] *Exynos 7 Octa (7870)*, SAMSUNG, http://www.samsung.com/semiconductor/minisite/Exynos/w/solution/mod_ap/7870/ (last visited Sep. 16, 2016); *Samsung Mass Produces 14-Nanometer Exynos Processor with Full Connectivity Integration*, SAMSUNG (Aug. 30, 2016), https://news.samsung.com/global/samsung-mass-produces-14-nanometer-exynos-processor-with-full-connectivity-integration ("Exynos 7570, with four Cortex-A53 cores in 14nm, delivers 70 percent improvements in CPU performance and 30 percent improvement in power efficiency when compared to its predecessor built on 28nm.").

[11] TECHINSIGHTS, 14 NM NODE SAMSUNG EXYNOS 7 7420 SOC (2016) at 28.

[12] *Id.* at xv; *see generally id*. at xvi-xviii.

[13] *Id.* at 17.

[14] Low, *supra* note 3; *Exynos 7 Octa (7420)*, SAMSUNG, http://www.samsung.com/semiconductor/minisite/Exynos/w/solution/mobile_ap/7420/ (last visited Sep. 8, 2016).

[15] TECHINSIGHTS, *supra* note 11, at xv ("Samsung's Exynos 7420 SoC [is] fabricated using Samsung's first generation bulk finFET technology at a 14 nm lithographic node."); *see also* TECHINSIGHTS at xvii ("Lightly doped bulk P-type silicon (Si) substrate."), 17 ("The device features a lightly doped p-type bulk silicon substrate having a <110> channel orientation, hafnium oxide/silicon oxide gate dielectric, dual band edge work function metal gates, tungsten contacts and metal 0, 10 levels of copper metallization, aluminum top metal (metal 11) redistribution layer and carbon-doped low-k dielectric (SiOC) inter-level dielectrics."), 19 ("The Samsung Exynos 7420 application processor is fabricated using a lightly doped bulk P-type monocrystalline Si substrate.").

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[16] *Exynos 7 Octa* (7420).

[17] TECHINSIGHTS at 71.

[18] *Id.* at xv; *see also id.* at 51 ("Three dimensional finFET with silicon fin, replacement metal gate (RMG) process and high-k dielectric are used for NMOS transistors."), 23 ("The Samsung Exynos 7420 uses shallow trench isolation (STI) to provide isolation between the fin structures (devices) on the die and the trenches are filled with a single oxide (SiO2). The Exynos 7420 adopts a two-step etch process to define the fins (1st shallower etch) and a second etch to define deeper STI trenches. The deeper isolation trenches are likely self-aligned to the sidewall edges of the adjacent finFET devices. Parasitic conduction path between finFET devices can be lowered by adoption of deeper STI since electrical isolation between devices is improved using this kind of deep isolation trenches. Pad oxide/nitride mask layers are likely used to pattern the trenches into the substrate, as is typical of most STI processes. A patterning of the fins likely uses a spacer-based double patterning. After completion of deeper STI formation, the trenches are filled with oxide (SiO2) and CMP planarized. The STI oxide fill is then etched back to expose the fins.").

[19] *Id.* at 19.

[20] *Strong 14nm FinFET Logic Process and Design Infrastructure for Advanced Mobile SOC Applications*, SAMSUNG (2013), http://www.samsung.com/us/samsungsemiconductor/pdfs/14nm-Foundry-032013.pdf.

[21] TECHINSIGHTS at 23-24, 88.

[22] *Id.* at 25-26 ("An additional etch process was likely used to form the top portions of the fins which are thinner with respect to the lower fin portions. This may have been achieved by oxidizing the fins, then stripping off the oxides to create the fins with narrower upper portions.").

[23] *Exynos 7 Octa (7420)*.

[24] TECHINSIGHTS at 71, 30 (respectively).

[25] *Id.* at 23 ("The Exynos 7420 adopts a two-step etch process to define the fins (1st shallower etch) and a second etch to define deeper STI trenches. The deeper isolation trenches are likely self-aligned to the sidewall edges of the adjacent finFET devices. Parasitic conduction path between finFET devices can be lowered by adoption of deeper STI since electrical isolation between devices is improved using this kind of deep isolation trenches. Pad oxide/nitride mask layers are likely used to pattern the trenches into the substrate, as is typical of most STI processes. A patterning of the fins likely uses a spacer-based double patterning."); *see also id.* at xvii ("1st shallow trench isolation (STI) used to define fin and additional deeper STI to provide better isolation between finFET devices. Single oxide (SiO2) is filled in defined STI and CMP planarization. Recess etch to expose sidewall of fin and form lateral shallow trench isolation, STI.").

[26] *Id.* at 40; *see also id.* at 17 ("The Samsung Exynos 7420 application processor . . . features a lightly doped p-type bulk silicon substrate having a <110> channel orientation, hafnium oxide/silicon oxide gate dielectric, dual band edge work function metal gates, tungsten contacts and metal 0, 10 levels of copper metallization, aluminum top metal (metal 11) redistribution layer and carbon-doped low-k dielectric (SiOC) inter-level dielectrics.").

[27] *Samsung-GlobalFoundries 14nm Collaboration*.

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[28] TECHINSIGHTS at 30, 69.

[29] *Id.* at 51; *see also id.* at 90 ("The I/O transistors of the Exynos 7420 share all the same processes and structures as their transistors in the logic region. In order to operate at a higher voltage, the I/O transistor employs a thicker silicon gate oxide (SiO2) while using the same high-k dielectric thickness as logic and larger gate length."), 241 ("High-k last HfO/SiO2 gate dielectric stack and dual gate oxide process between standard logic transistor, SRAM, and I/O transistor including other higher V_{th} transistors.").

[30] *Id.* at 40; *see also id.* at 241 ("High-k last HfO/SiO2 gate dielectric stack and dual gate oxide process between standard logic transistor, SRAM, and I/O transistor including other higher V_{th} transistors.").

[31] *Id.* at 40, 50.

[32] *Id.* at xv ("PMOS metal gate stacks consist of AlTiN work function adjustment layer, AlTiC, metal oxide (likely AlTiO), TiN capping layer and W gate filling metal. W is not filled in the narrow space of gate trenches in standard logic PMOS transistors including SRAM PMOS pull-up transistors. AlTiN PMOS work function layer is likely removed from NMOS transistors prior to depositing NMOS work function adjustment layer (AlTiC). NMOS metal gate stacks start with remnant AlTiN PMOS work function layer, AlTiC NMOS work function layer, metal oxide (likely AlTiO), TiN capping layer and W gate filling metal.").

[33] *Id.* at 40; *see also id.* at xv ("The finFET channel is oriented to the <110> directions with minimum gate length 27 nm for PMOS transistor and 30 nm for NMOS transistor in logic region. . . . The device features a 78 nm minimum observed contacted gate pitch, 49 nm minimum observed fin pitch and 0.08 μm2 minimum observed 6T SRAM cell area.").

[34] *Samsung-GlobalFoundries 14nm Collaboration*.

[35] TECHINSIGHTS at 28, 23 (respectively).

[36] *Id.* at xv ("Embedded SiGe in PMOS source/drain regions apply compressive strain to transistor P-channel to increase holes [*sic*] mobility and improve transistor performance."); *see also id.* at 40 ("Strain silicon techniques for stressing the transistor channels are employed including SEG (selective epitaxial growth) layers in the S/Ds such as embedded SiGe (eSiGe) in PMOS and embedded Si (eSi) in NMOS."), 100 ("The source and drain epitaxial layers are the same as the standard logic (eSi for NMOS and eSiGe PMOS).").

[37] *Id.* at 64; *see also id.* at 130 ("Contact to PMOS source/drain region is formed on an elevated SiGe island that is epitaxially grown in the recessed fin. Contact to NMOS source/drain region is formed on a raised Si island formed by epitaxial growth in the fin recess.").

[38] *Exynos 7 Octa (7420)*.

[39] TECHINSIGHTS at xv, 44.

[40] *Id.* at 17; *see also id*. at 40 ("The Samsung Exynos 7420 application processer [*sic*] is fabricated using Samsung's 1st generation finFET process technology in which a gate is wrapped around a thin three-dimensional silicon fin. The device employs multi-layered metal gates using a gate last process (RMG-replacement metal gate), epitaxial Si in the source/drains (S/D) of the NMOS finFETs and epitaxial silicon germanium (e-SiGe) in

EXHIBIT B
Infringement Chart for U.S. Patent No. 6,885,055

the PMOS S/Ds. Dual work function metal gates are used for PMOS and NMOS finFETs. A high-k dielectric including thin interface oxide separates the fin from the metal gate on each of the three sides of the fin. The gate dielectric consists of ~0.8 nm interface dielectric SiO2 and ~1.2 nm high-k dielectric HfO. The I/O transistor is observed to have a thicker interface dielectric SiO2 as compared to the standard logic transistor. The metal gates are constrained to be parallel in one direction (across the fin direction) and have a contacted gate pitch about 78 nm and minimum gate length of 27 nm for PMOS and 30 nm for NMOS in standard logic area."), 65 ("A stack of metal 0 (W) and contact (W) is used for contacting to source/drain eSi regions.").

[41] *Id.* at 72, 124.

[42] *Id.* at 40; *see also id*. at 241 ("High-k last HfO/SiO2 gate dielectric stack and dual gate oxide process between standard logic transistor, SRAM, and I/O transistor including other higher V_{th} transistors . . . 1.2 nm/0.8 nm (HfO/SiO2) in the core logic and SRAM transistors . . . 1.2 nm/3.8 nm (HfO/SiO2) in the higher voltage I/O transistors.").

[43] *Id.* at 50.

[44] *Id.* at 49.

[45] *Id.* at 28.

[46] *Id.* at 49.

[47] *Id.* at 28.

[48] *Id.* at 23 ("The Samsung Exynos 7420 uses shallow trench isolation (STI) to provide isolation between the fin structures (devices) on the die and the trenches are filled with a single oxide (SiO2). The Exynos 7420 adopts a two-step etch process to define the fins (1st shallower etch) and a second etch to define deeper STI trenches. The deeper isolation trenches are likely self-aligned to the sidewalls edges of the adjacent finFET devices. Parasitic conduction path between finFET devices can be lowered by adoption of deeper STI since electrical isolation between devices is improved using this kind of deep isolation trenches.").

[49] *Id.* at 119, 49 (respectively).

[50] *Id.* at 40; *see also id*. at xvii ("Pattern and expose NMOS S/D; etch to form silicon cavity; Si selective epitaxial growth (likely in-situ doped). Pattern and expose PMOS S/D; etch to form silicon cavity; SiGe selective epitaxial growth (likely in-situ doped), graded Ge concentration from top to bottom.").

[51] *Id.* at 64, 72, 47 (respectively).

[52] *Id.* at 40; *see also id*. at 130 ("Contact to NMOS source/drain region is formed on a raised Si island formed by epitaxial growth in the fin recess."), 47 ("Epitaxially formed e-Si regions are used in the NMOS source/drain regions."), 100 ("The source and drain epitaxial layers are the same as the standard logic (eSi for NMOS and eSiGe PMOS)."), 64 ("Source/drain regions of NMOS finFETs are anisotropically etched to form

recess in the fin and embedded Si (eSi) is formed by selective epitaxial growth. The shape of eSi is more rounded compared to the diamond shaped eSiGe in PMOS source/drain regions.").

[53] *Id.* at 40.

[54] *Id.* at 28; *see also id.* at 23 ("The fin thickness and fin pitches observed from both NMOS and PMOS device are likely uniform. Exposed fins are likely rounded and thinned. Rounding the fins improves transistor performance by reducing the probability of TDDB (time dependent dielectric breakdown) due to sharp corners and increased electric fields. Thinned fin might provide better electrostatic control from the metal gate.").

[55] *Id.* at 28, 30.

[56] *Id.* at 26.

[57] *Id.* at 27.

[58] *Id.* at 23.